IDEC Chip Design Contest

A Multi-Electrode Temporal Interference Stimulation (Multi-TIS) Driver IC

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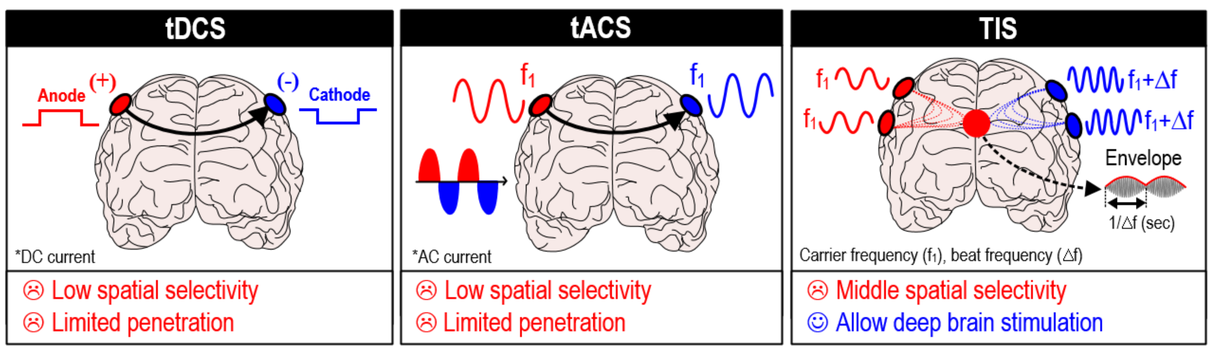
Abstract

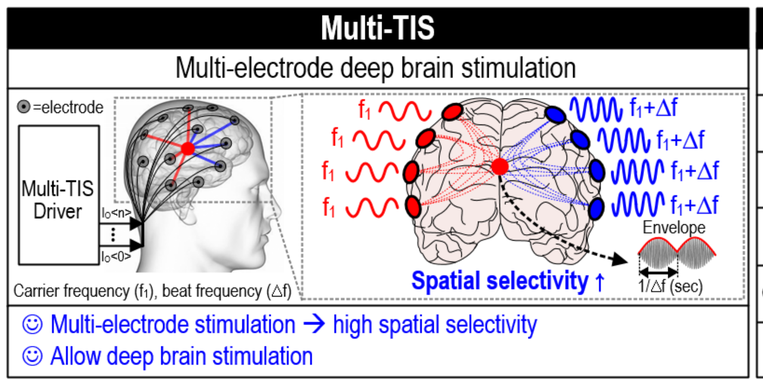
Surgical procedures and pharmacological treatments have been employed for the treatment of neurological disorders such as epilepsy, Parkinson's disease, and depression. However, these approaches are limited by high costs and potential surgical side effects. To overcome these limitations, non-invasive neuromodulation techniques are proposed. This paper presents a multi-electrode temporal interference stimulation (Multi-TIS) , enabling precise non-invasive deep brain stimulation. Fabricated in a 180 nm BCD process, the IC delivers stable ± 1 mA output current across 15 kΩ loads.

Operation principles of tDCS,tACS,TIS



The non-invasive neuromodulation techniques such as transcranial direct current stimulation (tDCS) and transcranial alternating current stimulation (tACS) have gained attention. Nonetheless, tDCS suffers from shallow penetration depth due to rapid signal attenuation in brain tissue, while tACS provides limited spatial resolution, particularly for deep brain regions. Temporal Interference Stimulation (TIS) has recently emerged as a promising alternative, capable of overcoming these inherent limitations.

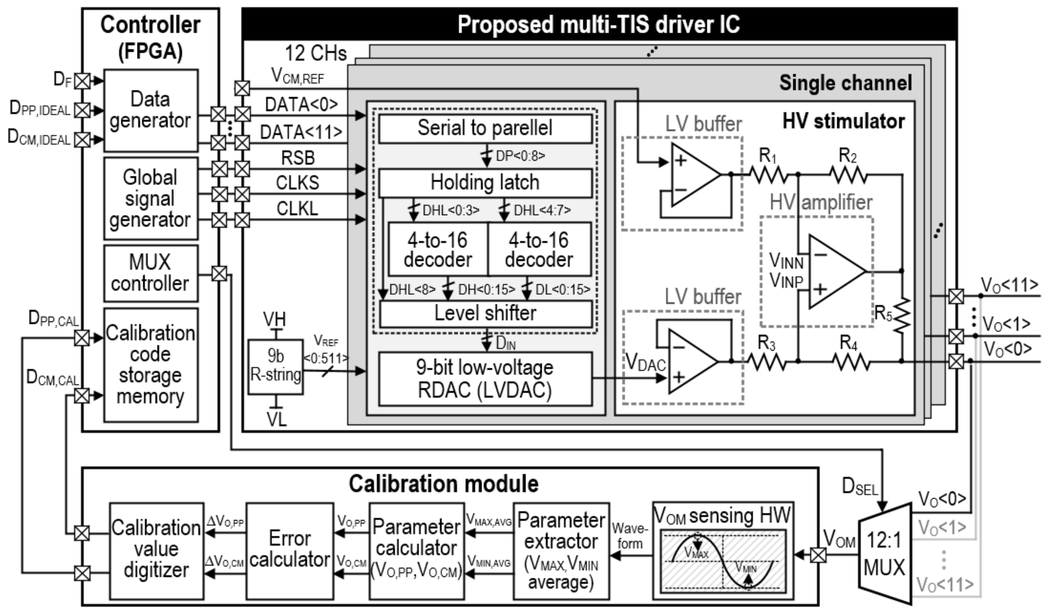
Multi-Temporal Interference Stimulation (Multi-TIS) System



Comparison multi-TIS & TIS		
Comparison	Multi-TIS	TIS
Min. number of electrodes	6	4
Min. number of driving signals	6	4
Spatial selectivity	High	Middle
Cortical stimulation reduction	Effective	Limit
Number of simultaneously activated electrodes	6	4

Temporal Interference Stimulation (TIS) employs four electrodes to deliver stimulation by generating an envelope waveform through the superposition of two in-phase sine waves and two anti-phase sine waves, using a single carrier frequency and a delta frequency. Compared to TIS, Multi-TIS introduces two additional electrodes, enabling more precise targeting of the stimulation site through enhanced spatial resolution

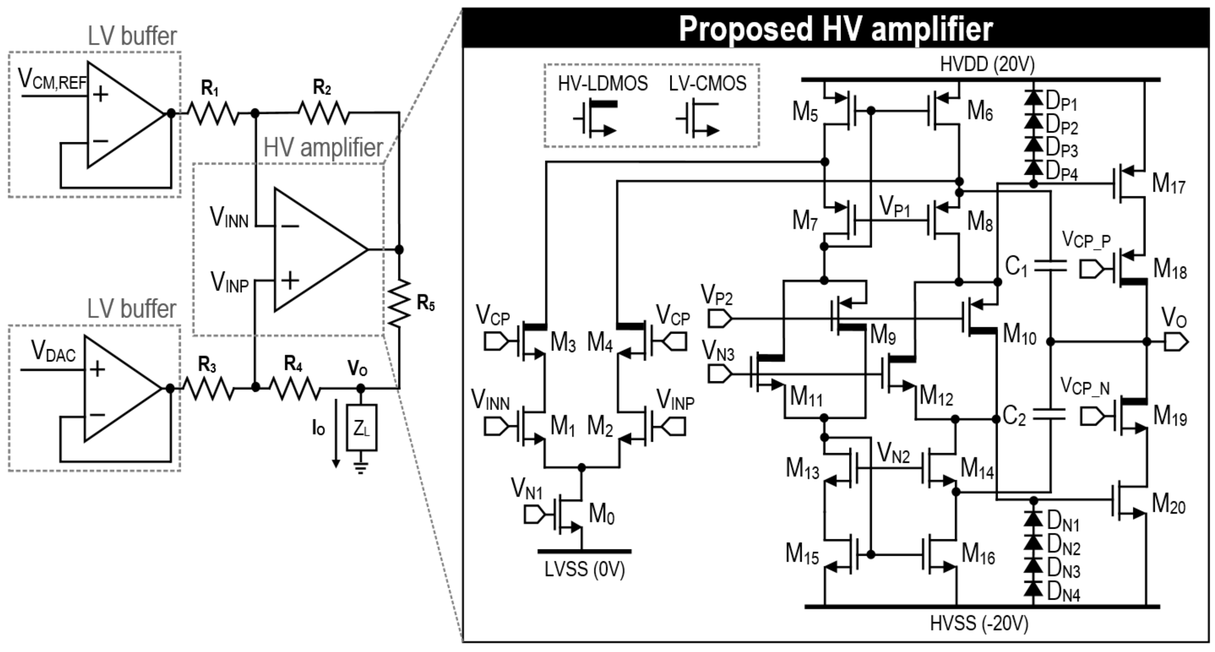
Proposed Multi-TIS Drive IC Architecture



The multi-TIS system architecture, consisting of the multi-TIS driver IC, FPGA controller, and a calibration module. A 9-bit serial data stream from the FPGA is converted into parallel form, followed by DAC to produce a sinusoidal waveform. The resulting signal is amplified by a high-voltage (HV) stimulator for target signals.

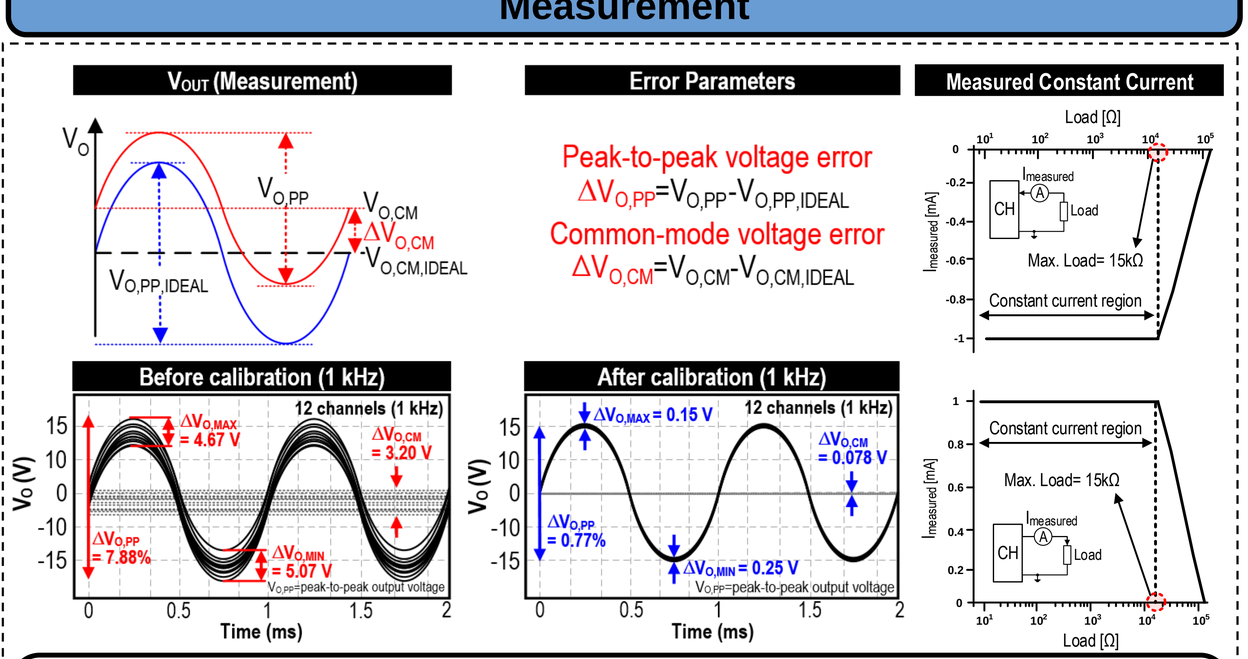
Proposed Channel Circuit with Howland Current Pump(HCP)

– 1CH –



The three key parameters of the HCP are the scale of the resistors used, the feedback ratio, and the value of the current sensing resistor(R_5).

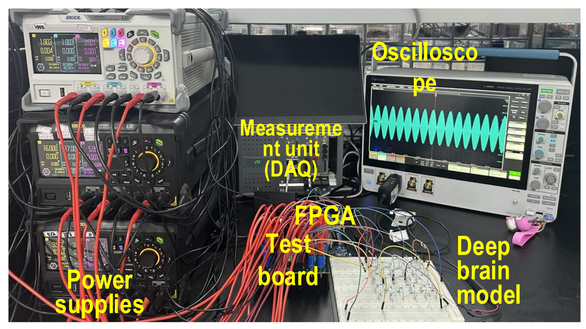
Concept of the Proposed Mismatch-Calibration and Measurement



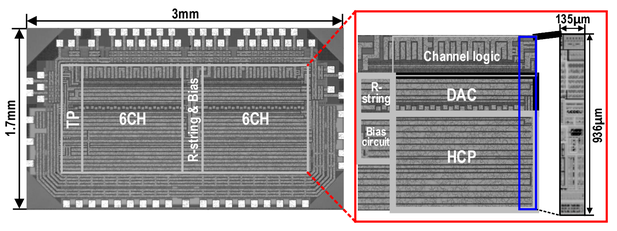
Measured output current under ±1 mA target across 15 kΩ loads at 1kHz. The uncalibrated outputs exhibit a $\Delta V_{O,PP}$ of 7.88 % and a $\Delta V_{O,CM}$ of 3.2 V. With calibration applied, these values are reduced to 0.77 % and a 78 mV. These results confirm significantly improving channel uniformity.

Overview of Fabricated Chip and Conclusion

Measurement Setup



Die Micrograph



The proposed multi-TIS driver IC was fabricated using a 180 nm BCD process. Above figure shows the measurement setup and die micrograph. It presents a new multi-TIS driver IC which is consists of a total of 12 channels, capable of driving current up to 2mA, and supports measurements at carrier frequency up to 10kHz. A calibration scheme effectively compensates for $\Delta V_{O,PP}$ and $\Delta V_{O,CM}$, improving channel uniformity.

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